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Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA

Bishwajeet Pandey[1], Md. Atiqur Rahman[1], Dil M. Akbar Hussain[2], Abhay Saxena[3] and Bhagwan Das[4]

[1]Gyancity Research Lab, India; gyancity@gyancity.com, atiqur.rahman.mim@gmail.com
[2]Aalborg University, Denmark; akh@et.aau.dk
[3]Dev Sanskriti Vishwavidyalaya, Haridwar, India; abhaysaxena2009@gmail.com
[4]UTHM, Malaysia; engr.bhagwandas@hotmail.com

Abstract

The 8-bit design is able to process 256 times input combination in compare to 4-bit vedic multiplier, using approximates 6 times basic elements, 2 times IO buffers, approximate 1.5 times total power dissipation. HSTL_I_12, SSTL18_I and LVCMOS12 are the most energy efficient IO standards in HSTL, SSTL and LVCMOS family respectively. Device static power and design static power are two types of static power dissipation. Device static power is also known as Leakage power when the device is on but not configured. Design static power is power dissipation when bit file of design is downloaded on FPGA but there is no switching activity. Design static power dissipation of 8-bit Vedic multiplier is almost double of design static power dissipation of 4-bit Vedic multiplier. Device static (leakage) power dissipation of 8-bit Vedic multiplier is almost equal to device static power dissipation of 4-bit Vedic multiplier on 40nm FPGA.

Keywords: HSTL, IO Standards, LVCMOS, SSTL, Static Power Reduction, Vedic Multiplier, Voltage Scaling

1. Introduction

The Input Output Standard (IOSTANDARD) constraint is both mapping constraint and synthesis constraint. Modern Programmable Logic Devices (PLDs), such as Field Programmable Gate Arrays (FPGAs), are capable of supporting a variety of different input/output (I/O) standards from 29 logic families as shown in Table 1. In this work, three different logic families out of 29 different available logic families on FPGA are used. These are Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS), Stub Series Terminated Logic (SSTL) and High Speed Terminated Logic (HSTL). In LVCMOS family, LVCMOS12 is delivering best power specific performance and LVCMOS25 is delivering worst power specific performance out of different IO standards available in LVCMOS family[1,3,4]. In HSTL family, HSTL_I_12 is delivering best power specific performance and HSTL_I_DCI_18 is delivering worst power specific performance out of different IO standards available in HSTL family[3,4]. In SSTL family, SSTL18_I is delivering best power specific performance. SSTL2_II_DCI (SSTL2_D) is delivering worst power specific performance out of different IO standards available in SSTL family[4].

XC4000 FPGA was based on 500nm technology which uses 5V supply voltage. Supply voltage reduces to 3.3V with Spartan-XL FPGA family. Supply voltage of FPGA again reduces to 2.5V with Virtex FPGA family. With 40nm technology based FPGA, supply voltage is in range of -0.5V to 1.1V as shown in Table 1.

**Author for correspondence*

Table 1. Evolution of FPGA

FPGA	Technology	Supply Voltage
XC4000	500nm	5V
Spartan	350nm	5V
XL	250nm	3.3V
Spartan-II	220nm	2.5V
Virtex	220nm	2.5V
Virtex-E	180nm	1.8V
Virtex-II	150nm	1.5V
Virtex-II Pro	130nm	1.5V
Virtex-4	90nm	-0.500 to 1.32V
Virtex-5	65nm	–0.500 to 1.1V
Virtex-6	40nm	–0.500 to 1.1V
Virtex-7	28nm	–0.500 to 1.1V
Virtex Ultra Scale FPGA	20nm	–0.500 to 1.1V

1.1 Applicable Elements

IO standard is applicable in Verilog Code, VHSIC Hardware Description Language (VHDL) code, User Constraint File (UCF), Physical Constraint File (PCF) file and Xilinx Constraint File (XCF). Target design is multiplier because multiplier is widely used in wireless communication. For energy efficient wireless communication, there is need to design energy efficient multiplier. Both CMOS 65 nm sigma delta frequency synthesizer and embedded capacitor multiplier has gigabit baseband rate for millimeter wave communication[9]. The capacitor multiplier achieves an equivalent value of 540 pF and save 90% area for main capacitor[9]. A multiplier circuit and wireless communication apparatus that adjust an output level of a desired multiple waves to a desired range are discussed in[10]. An apparatus for receiving signals includes a Low Noise Amplifier (LNA) configured to receive a Radio Frequency (RF) signal is using 16 multipliers[11]. A high speed low power digital multiplier by taking the advantage of Vedic multiplication algorithms with a very efficient leakage control technique called McCMOS technology is designed[12]. This work is extension of McCMOS technology to LVCMOS, HSTL and SSTL IO standards available on 40nm process technology to control both device static and design static power.

3. Top Level Schematic of Vedic Multiplier

The top level schematic of 8-bit Vedic multiplier that is based on the Vedic formula called *Urdhva Triyagbhyam*. Figure 1 is top level schematic of 8-bit Vedic Multiplier (VM). Let Register Transfer Language (RTL) is the impedance for transmission line, RIO is the impedance for IO Ports and RALU is the impedance for the target circuit of VM, then after applying suitable IO standard, all three impedance will be equal as shown in equation (1).

$$RTL = RIO = RVM \tag{1}$$

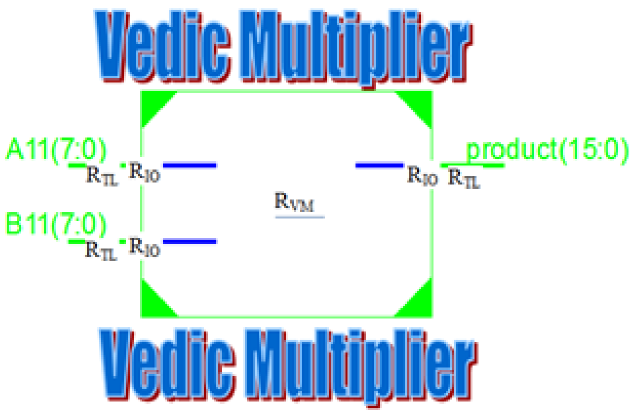

Figure 1 Top Level Schematic of 8-bit Vedic Multiplier.

2.1 RTL Schematic of Vedic Multiplier

This 8-bit Vedic multiplier is using four 4-bit Vedic multiplier and three 8-bit full adders as shown in Figure 2. LAB1, LAB2, LAB3, and LAB4 are four instance of 4-bit Vedic multiplier. FA11, FA12 and FA13 are three instance of full adder. Inputs are A11 [7:0] and B11 [7:0]. Output is product [15:0].

2.1.1 Logic Utilization

Four-bit Vedic multiplier can multiply 256 combination of two 4-bit input from 0x0 to 15x15. Eight-bit Vedic multiplier can multiply 65536 combination of two 8-bit input from 0x0 to 256x256. The 8-bit design is taking 256 time input combination, whereas using approximates 6 times basic elements and 2 times IO buffers.

4-Bit Vedic Multiplier is using 26 basic elements in compare to 153 basic elements in 8-bit Vedic multiplier. LUTN represents N-bit LUT. LUT2, LUT3, LUT4, LUT5, and LUT6 are five different LUT available in 40nm technology based Virtex-6 FPGA. There is no LUT3 and LUT5 in 4-bit Vedic multiplier. In 8-bit Vedic multiplier, Xilinx Synthesis Technology (XST) is using all 5 different LUTs. There are 50% less IO Buffers, 90.91% less LUT2, 100% less LUT3, 73.81% less LUT4, 100% less LUT5, and 80.56% less LUT6 used in 4-bit Vedic multiplier in compare to 8-bit Vedic multiplier as shown in Table 2.

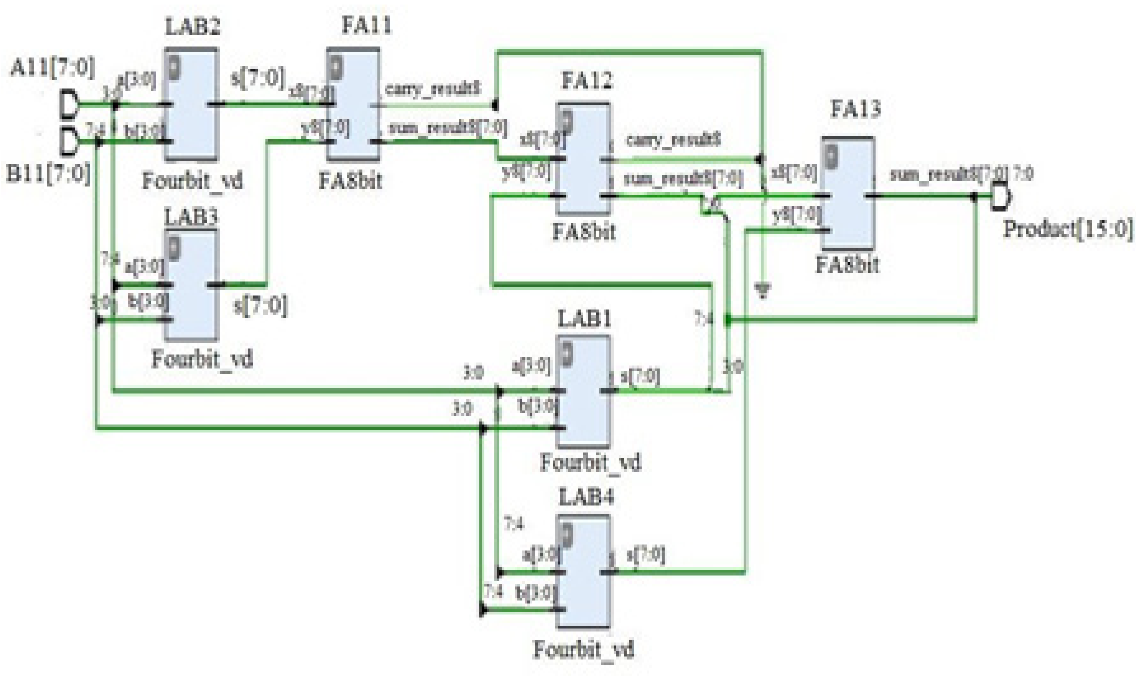

Figure 2. RTL Schematic of Vedic Multiplier.

Table 2. Logic Utilization of 4-Bit Vedic Multiplier and 8-bit Vedic Multiplier

	4-Bit Vedic Multiplier	8-bit Vedic Multiplier
BELS	26	153
LUT2	1	11
LUT3	-	2
LUT4	11	42
LUT5	-	26
LUT6	14	72
IO Buffers	16	32
IBUF	8	16
OBUF	8	16

2.1.2 Power Dissipation on FPGA

Total FPGA power = Device Static + Design Static + Design Dynamic

Dynamic powers are modeled to account for load capacitance, supply voltage, and operating frequency. In this paper, primary concern is analysis and reduction of static power. There are two types of static power. One is device static power and other is design static power. Device static power is also known as Leakage power when the device is powered and not configured. Device static power is mainly sensitive to ambient temperature. Design static power is additional power dissipation when the device is configured but there is no switching activity. Design static power includes static power in I/O DCI terminations, clock managers, etc.

3. Working of Vedic Multiplier Based on Urdhva-Tiryagbhyam Sutra in Vedic Mathematics

Urdhva-Tiryagbhyam means vertically and column wise.

Let's consider a case of multiplication of 24 by 34.

Step 1: Multiply 2 with 3 (Vertically)

Step 2: Multiply 4 with 4. (Vertically)

Step 3: Multiply (2*4) and (4*3) (column wise) and add these (8+12).

Step 4: Write 6 out of 16 generated in Step 2.

Step 5: Add carry 1 generated in Step 4 to 20 generated in Step 3.

Step 6: Write 1 out of 21 generated in Step 5. Carry 2 for next step.

Step 7: Add Carry 2 into 6 generated in step 1. And write 8 at Maximum significant digit.

Step 8: Final result is 816.

4. Power Analysis of 8-bit Vedic Multiplier on 40nm FPGA

In power analysis, SSTL2_D for SSTL2_II_DCI and HSTL_D18 for HSTL_I_DCI_18 is used. Any 8-bit multiplier can multiply 0x0, 0x1,......0x15,....1x3,....1x15,.....2x 15,....15x15,.........255x255. It can covers 65,536 combination of two 8-bit inputs. Final result is 16-bit output.

Table 3. Examples of *Urdhva Triyagbhyam*

00001110 00001110	00011000 00100010	00010110 00001100	00010111 00001100
14 14	24 34	22 12	23 12
(1*1)(1*4+4*1)(4*4)	(2*3)(2*4+4*3)(4*4)	(2*1)(2*2+2*1)(2*2)	(2*1)(2*2+3*1)(3*2)
296	816	264	276
0000000100101000	0000001100110000	0000000100001000	0000000100010100

Table 4. Total Power Dissipation on 40nm FPGA

Volt	LVCMOS12	LVCMOS25	HSTL_I_12	HSTL_D18	SSTL18_I	SSTL2_D
0.5V	0.739W	0.740W	1.003W	1.299W	1.021W	2.404W
1.0V	1.291W	1.293W	1.575W	1.877W	1.593W	3.004W
1.2V	2.076W	2.078W	2.374W	2.684W	2.393W	3.845W
1.5V	5.623W	5.625W	5.975W	6.333W	5.996W	7.677W

Table 5. Device Static (Leakage) Power Dissipation on 40nm FPGA

Volt	LVCMOS12	LVCMOS25	HSTL_I_12	HSTL_D18	SSTL18_I	SSTL2_D
0.5V	0.739W	0.740W	0.739W	0.741W	0.740W	0.744W
1.0V	1.291W	1.293W	1.298W	1.305W	1.299W	1.331W
1.2V	2.076W	2.078W	2.091W	2.107W	2.092W	2.167W
1.5V	5.623W	5.625W	5.684W	5.747W	5.688W	5.991W

Table 6. Design Static Power Dissipation on 40nm FPGA

Volt	LVCMOS12	LVCMOS25	HSTL_I_12	HSTL_D18	SSTL18_I	SSTL2_D
0.5V	NA	NA	0.264W	0.559W	0.281W	1.659W
1.0V	NA	NA	0.277W	0.572W	0.295W	1.673W
1.2V	NA	NA	0.283W	0.577W	0.300W	1.678W
1.5V	NA	NA	0.291W	0.585W	0.308W	1.686W

SSTL is dissipating more power among 3 different family of IO standards. Whereas, LVCMOS is the most power optimized IO standards available on 40nm FPGA as shown in Table 6. There is 69.26%, and 58.28% reduction in power dissipation when LVCMOS, and HSTL is used in place of SSTL on 0.5Volt. When supply voltage increases then the difference in power dissipation is decreases. There is only 26.76%, 22.17% reduction in power dissipation when LVCMOS12, HSTL_I_12 in place of SSTL2_D on 1.5Volt is used.

Device static power is also known as leakage power. Leakage power is not significantly affected with variation in IO standards of either same or different IO standard family. Using SSTL or LVCMOS12, there is 6.14% change in power dissipation at 1.5V and 0.67% change in power dissipation at 0.5V as shown in Table 7. When supply voltage is scale down from 1.5V to 0.5V, then there is 86.84%, 87.11% and 87.58% reduction in leakage power for LVCMOS25, HSTL_D18 and SSTL2_D as shown in Table 5.

When using HSTL_I_12, SSTL18_I, HSTL_D18 in place of SSTL2_D then there is 84.09%, 83.06%, and 66.31% reduction in design static power dissipation of Vedic multiplier at 0.5V supply voltage as shown in Table 8. There is less effect of voltage scaling on power reduction. Similar reduction in power (percentage) with variation in IO standard on 1.0V, 1.2V and 1.5V is observed as observed on 0.5V. There is 26-27mW reduction in power for both HSTL and SSTL IO standard as shown in Table 6.

5. Power Analysis of 4-bit Vedic Multiplier on 40nm FPGA

A 4-bit multiplier can multiply 0x0, 0x1,......0x15,....1x3,....1x15,.....2x15,....15x15. It can covers 256 combination of two 4-bit inputs. Final result is 8-bit output.

Using LVCMOS12, LVCMOS25, HSTL_I_12, HSTL_D18, and SSTL18_I in place of SSTL2_D, then there is 52.99%, 52.93%, 44.59%, 35.18% and 44.02% reduction in total power dissipation on 40nm FPGA and 0.5V supply voltage as shown in Table 9. When LVCMOS12, LVCMOS25, HSTL_I_12, HSTL_D18, and SSTL18_I is used in place of SSTL2_D, then there is 15.41%, 15.38%, 12.76%, 10.06% and 12.59% reduction in total power dissipation on 40nm FPGA and 1.5V supply voltage as shown in Table 7.

As shown in Table 8, when supply voltage is scaled down from 1.5V to 0.5V, then there is 86.86%, 86.84%, 86.93%, 86.98%, 86.93%, and 87.22% reduction in device static (leakage) power for LVCMOS12, LVCMOS25, HSTL_I_12, HSTL_D18, SSTL18_I and SSTL2_D respectively. There is 0.4%, 1.6%, 2.17% and 3.12% reduction in leakage power when we use LVCMOS12 in place of SSTL2_D at 0.5V, 1.0V, 1.2V and 1.5V respectively.

There is 84.1%, 83.01%, and 66.39% reduction in design static power dissipation of Vedic multiplier when we use HSTL_I_12, SSTL18_I, HSTL_D18 in place of SSTL2_D at 0.5V supply voltage as shown in Table 9.

Table 7. Total Power Dissipation on 40nm FPGA

Volt	LVCMOS12	LVCMOS25	HSTL_I_12	HSTL_D18	SSTL18_I	SSTL2_D
0.5V	0.739W	0.740W	0.871W	1.019W	0.880W	1.572W
1.0V	1.291W	1.293W	1.433W	1.584W	1.443W	2.148W
1.2V	2.076W	2.078W	2.225W	2.380W	2.235W	2.961W
1.5V	5.623W	5.625W	5.799W	5.978W	5.810W	6.647W

Table 8. Device Static (Leakage) Power Dissipation on 40nm FPGA

Volt	LVCMOS12	LVCMOS25	HSTL_I_12	HSTL_D18	SSTL18_I	SSTL2_D
0.5V	0.739W	0.740W	0.739	0.740	0.739	0.742
1.0V	1.291W	1.293W	1.295	1.298	1.295	1.312
1.2V	2.076W	2.078W	2.084	2.092	2.085	2.122
1.5V	5.623W	5.625W	5.653	5.685	5.656	5.804

Table 9. Design Static Power Dissipation on 40nm FPGA

Volt	LVCMOS12	LVCMOS25	HSTL_I_12	HSTL_D18	SSTL18_I	SSTL2_D
0.5V	NA	NA	0.132W	0.279W	0.141W	0.830W
1.0V	NA	NA	0.139W	0.286W	0.147W	0.836W
1.2V	NA	NA	0.141W	0.289W	0.150W	0.839W
1.5V	NA	NA	0.145W	0.293W	0.154W	0.843W

6. Power Analysis of Scaling of Vedic Multiplier on 40nm FPGA

6.1 For LVCMOS IO Standard

When voltage is varied from 1.5V to 1.2V, 1.0V and 0.5V, then there is 63.08%, 77.04%, and 86.86% saving in total power dissipation respectively for LVCMOS12 IO standards available on 40nm FPGA. With LVCMOS25, similar saving in power dissipation as with LVCMOS12 is analyzed as shown in Table 10. With LVCMOS IO standard, power dissipation for both 4-bit and 8-bit Vedic multiplier is same.

6.1.1 Data Collection Phase

HSTL IO standard is used in both 4-bit Vedic multiplier and 8-bit Vedic multiplier. With HSTL_I_12, 8-bit Vedic multiplier is using just 13.16% more power dissipation in compare to 4-bit Vedic multiplier whereas it is processing 99.61% more input combination (65536 combinations) than 4-bit vedic multiplier (256 combinations) as shown in Table 11.

For 8-bit Vedic multiplier and HSTL_I_12 IO standard, there is 63.21%, 77.09% and 86.93% reduction in leakage power when supply voltage is scaled down from 1.5V to 1.2V, 1.0V and 0.5V respectively as shown in Table 12.

Table 10. Total Power Dissipation of Vedic Multiplier Using LVCMOS on 40nm FPGA

	4-Bit Vedic Multiplier		8-Bit Vedic Multiplier	
Volt	LVCMOS12	LVCMOS25	LVCMOS12	LVCMOS25
0.5V	0.739W	0.740W	0.739W	0.740W
1.0V	1.291W	1.293W	1.291W	1.293W
1.2V	2.076W	2.078W	2.076W	2.078W
1.5V	5.623W	5.625W	5.623W	5.625W

Table 11. Total Power Dissipation of Vedic Multiplier Using HSTL on 40nm FPGA

	4-Bit Vedic Multiplier		**8-Bit Vedic Multiplier**	
Volt	**HSTL_I_12**	**HSTL_D18**	**HSTL_I_12**	**HSTL_D18**
0.5V	0.871W	1.019W	1.003W	1.299W
1.0V	1.433W	1.584W	1.575W	1.877W
1.2V	2.225W	2.380W	2.374W	2.684W
1.5V	5.799W	5.978W	5.975W	6.333W

Table 12. Device Static (Leakage) Power of Vedic Multiplier Using HSTL on 40nm FPGA

	4-Bit Vedic Multiplier		**8-Bit Vedic Multiplier**	
Volt	**HSTL_I_12**	**HSTL_D18**	**HSTL_I_12**	**HSTL_D18**
0.5V	0.739W	0.740W	0.739W	0.741W
1.0V	1.295W	1.298W	1.298W	1.305W
1.2V	2.084W	2.092W	2.091W	2.107W
1.5V	5.653W	5.685W	5.684W	5.747W

Table 13. Design Static Power Dissipation of Vedic Multiplier Using HSTL on 40nm FPGA

	4-Bit Vedic Multiplier		**8-Bit Vedic Multiplier**	
Volt	**HSTL_I_12**	**HSTL_D18**	**HSTL_I_12**	**HSTL_D18**
0.5V	0.132W	0.279W	0.264W	0.559W
1.0V	0.139W	0.286W	0.277W	0.572W
1.2V	0.141W	0.289W	0.283W	0.577W
1.5V	0.145W	0.293W	0.291W	0.585W

Design static power dissipation of 8-bit vedic multiplier is almost double of design static power dissipation of 4-bit vedic multiplier as shown in Table 13. In 8-bit vedic multiplier, when supply voltage is varied from 1.5V to 1.2V, 1.0V and 0.5V, then there is 2.75%, 4.81%, 9.28% saving in design static power with HSTL_I_12 and 1.36%, 2.22%, 4.44% saving in design static power with HSTL_D18.

6.2 SSTL IO Standards

With SSTL18_I and SSTL2_D IO standards, 8-bit Vedic multiplier is taking only 13.81% and 34.61% more power dissipation than 4-bit Vedic multiplier whereas data width of 8-bit Vedic multiplier is almost double of 4-bit Vedic multiplier on 0.5V supply voltage. For energy efficient SSTL18_I IO standards among SSTL family, 82.97%, 73.43% and 60.09% reduction in power dissipation with 0.5V in compare to 1.5V, 1.2V and 1.0V supply voltage respectively is achieved as shown in Table 14.

Device static (leakage) power dissipation of 8-bit Vedic multiplier is almost equal to device static power dissipation of 4-bit Vedic multiplier on 40nm FPGA. For 8-bit Vedic multiplier and SSTL2_D IO standards, we are saving 63.83%, 77.78%, and 87.58% power when supply voltage is varied from 1.5V to 1.2V, 1.0V and 0.5V respectively as shown in Table 15.

Table 14. Total Power Dissipation of Vedic Multiplier Using SSTL on 40nm FPGA

	4-Bit Vedic Multiplier		8-Bit Vedic Multiplier	
Volt	**SSTL18_I**	**SSTL2_D**	**SSTL18_I**	**SSTL2_D**
0.5V	0.880W	1.572W	1.021W	2.404W
1.0V	1.443W	2.148W	1.593W	3.004W
1.2V	2.235W	2.961W	2.393W	3.845W
1.5V	5.810W	6.647W	5.996W	7.677W

Table 15. Device Static (Leakage) Power of Vedic Multiplier Using SSTL on 40nm FPGA

	4-Bit Vedic Multiplier		8-Bit Vedic Multiplier	
Volt	**SSTL18_I**	**SSTL2_D**	**SSTL18_I**	**SSTL2_D**
0.5V	0.739W	0.742W	0.740W	0.744W
1.0V	1.295W	1.312W	1.299W	1.331W
1.2V	2.085W	2.122W	2.092W	2.167W
1.5V	5.656W	5.804W	5.688W	5.991W

Table 16. Design Static Power of Vedic Multiplier Using SSTL on 40nm FPGA

	4-Bit Vedic Multiplier		8-Bit Vedic Multiplier	
Volt	SSTL18_I	SSTL2_D	SSTL18_I	SSTL2_D
0.5V	0.141W	0.830W	0.281W	1.659W
1.0V	0.147W	0.836W	0.295W	1.673W
1.2V	0.150W	0.839W	0.300W	1.678W
1.5V	0.154W	0.843W	0.308W	1.686W

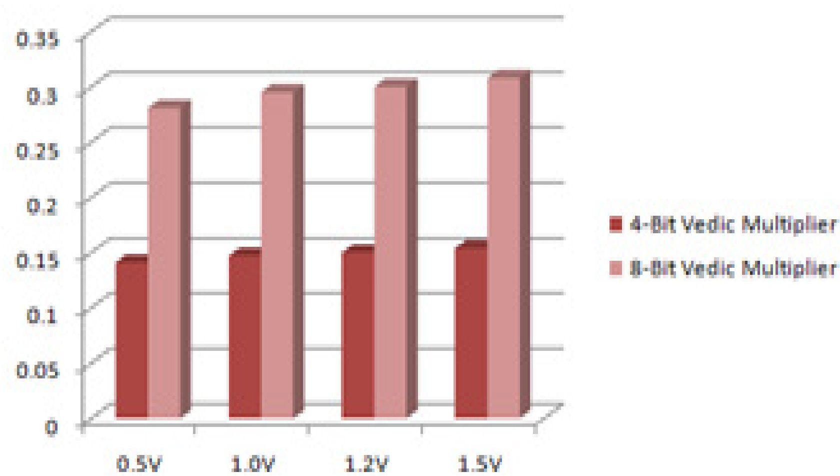

Figure 3. Comparison of Design Static Power Dissipation for SSTL18_I.

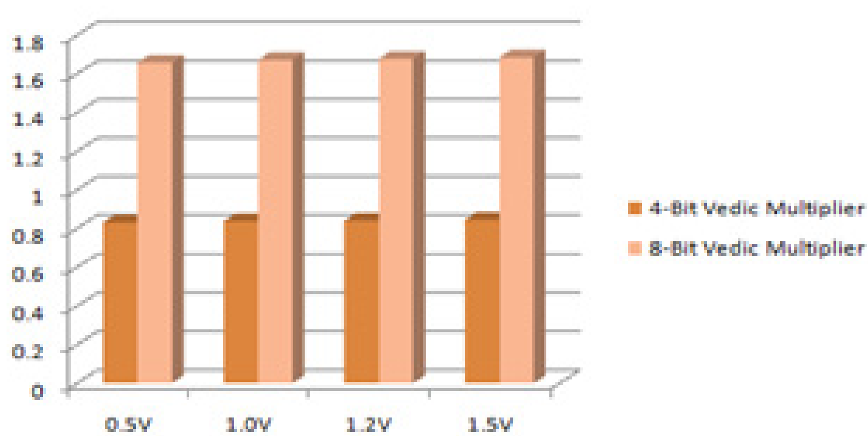

Figure 4. Comparison of Design Static Power Dissipation for SSTL2_D.

Design static power of 8-bit Vedic multiplier is almost double of design static power dissipation of 4-bit Vedic multiplier as shown in Table 16.

For SSTL18_I IO standard, when we scale down supply voltage from 1.5V to 1.2V, 1.0V and 0.5V then there is 2.6%, 4.22% and 8.76% reduction in design static power dissipation respectively.

When SSTL18_I is used in place of SSTL2_D, then there is 83.06%, 82.36%, 82.12% and 81.73% reduction in design static power at 0.5V, 1.0V, 1.2V and 1.5V respectively.

7. Conclusion

Eight-bit Vedic multiplier multiply 65536 combination of two 8-bit input from 0x0 to 256x256 which is more than 256 combination of 4-bit input from 0x0 to 15x15 for 4-bit Vedic multiplier. Our 8-bit design is able to process 256 times more input combination in compare to 4-bit vedic multiplier, whereas using only 6 times basic elements, 2 times IO buffers, approximate 1.5 times total power dissipation and 2 times design static power dissipation. HSTL_I_12, SSTL18_I and LVCMOS12 are the most energy efficient IO standards in HSTL, SSTL and LVCMOS family. Device static power and design static power are main component of static power dissipation. Both 4-bit and 8-bit Vedic multipliers are implemented on 40nm FPGA. When voltage is scaled down from 1.5V to 1.2V, 1.0V and 0.5V, then there is 63.08%, 77.04%, and 86.86% saving in total power dissipation respectively for LVCMOS12 IO standard. With HSTL_I_12, 8-bit vedic multiplier is using just 13.16% more power dissipation in compare to 4-bit vedic multiplier whereas it is processing 99.61% more input combination (65536 combinations) than 4-bit vedic multiplier (256 combinations). Design static power dissipation of 8-bit vedic multiplier is almost double of design static power dissipation of 4-bit vedic multiplier. Device static (leakage) power dissipation of 8-bit Vedic multiplier is almost equal to device static power dissipation of 4-bit Vedic multiplier. For 8-bit Vedic multiplier and SSTL2_D IO standards, we are saving 63.83%, 77.78%, and 87.58% device static power when supply voltage is scaled down from 1.5V to 1.2V, 1.0V and 0.5V respectively.

8. Future Scope

This design is implemented on 40nm technology based FPGA. In future, this design can be re-implemented on 28nm FPGA and 20nm ultra scale FPGA. This design of 8-bit Vedic multiplier can be extended as 16-bit Vedic multiplier and 32-bit Vedic multiplier. There is also open scope to integrate this multiplier in existing ALU and FIR filter and make a design of Vedic ALU, Vedic FIR Filter, and Vedic Math Co-processor. Here, we are using LVCMOS, HSTL and SSTL IO standards. There is wide scope to for other IO standards like High Speed Unterminated Logic (HSUL), Gunning Transceiver Logic (GTL), Peripheral Component Interconnect (PCI), Low Voltage Transistor Transistor Logic (LVTTL), Point-to-Point Differential Signaling (PPDS), Low Voltage Positive Emitter Coupled Logic (LVPECL), and Pseudo Open Drain (POD) Logic Standards and Lighting Data Transport (LDT).

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